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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/711,843

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Kevin Lin

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EXAMINER

ELAND, SHAWN

ART UNIT

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/711,843	<b>Applicant(s)</b> LIN, KEVIN	
	<b>Examiner</b> SHAWN ELAND	<b>Art Unit</b> 2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 28 October 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-4,6-9,11-15 and 18-24 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-4,6-9,11-15 and 18-24 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)            | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | Paper No(s)/Mail Date. _____                                      |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>11/04/08</u> .  | 6) <input type="checkbox"/> Other: _____                          |

### **DETAILED ACTION**

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/28/08 has been entered.

### ***Status of Claims***

Claims 1 – 4, 6 – 9, 11 – 15, & 18 – 24 are pending in the Application.

Claims 1, 6, 12, & 20 have been amended.

Claims 5, 10, & 16 – 17 are cancelled.

Claims 1 – 4, 6 – 9, 11 – 15, & 18 – 24 are rejected.

### ***Claim Objections***

Claim 24 is objected to because of the following informalities: “The method” in line 1 does not have proper antecedent basis. Appropriate correction is required.

### ***Response to Amendments***

Applicant's arguments with respect to claims 1, 6, 12, & 20 have been considered but are moot in view of the new ground(s) of rejection.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1 – 4, 6 – 9, 11 – 15, & 18 – 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Michigami*** (US 6,223,322) in view of ***Hennessey*** (“Computer Architecture A Quantitative Approach”, 1996).

In regard to claim 1, Michigami teaches generating a block index for a block of data the block index having a block index value (***figure 5 “LOGICAL MAPPING”***; ***Table 1***); mapping the block index to a physical address of a memory based on the block index value and a number N, wherein N is the number of banks of the memory (***figure 5***) wherein the mapping makes each one of the block indexes map in turns to one physical address located at different banks so that any adjacent block of data is stored physically at different banks of the memory (***col. 6, lines 32 – 44***); storing the block of data into the memory at the physical address (***figure 5 “PHYSICAL MAPPING”***).

In regard to claim 20, Michigami teaches generating a plurality of block indexes for a plurality of blocks of data (***figure 5 “LOGICAL MAPPING”***); mapping the block indexes sequentially to a plurality of physical address of a memory based on the block indexes and a number N, wherein N is a number of banks of the memory (***figure 5***) wherein the mapping comprises; dividing the block index value by N to obtain a quotient

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Q and a remainder R (**col. 6, lines 32 – 44**); and calculating the physical address based on Q and R, wherein the physical address is calculated as the result of  $Q \times \text{block\_size} + R \times \text{bank\_size}$ , wherein bank\_size equals the memory size divided by N, and block\_size equals the size of which the system is in need to process one sector from the optical disc (**figure 5**); and storing the block of data into the memory at the physical address (**figure 5 “PHYSICAL MAPPING”**); wherein the mapping makes each one of the block indexes map in turns to one physical address located at different banks so that any logical adjacent block of data be stored physically at different banks of the memory (**col. 6, lines 32 – 44**).

In regard to claim 6, Michigami teaches retrieving a block of data from a source medium (**Abstract**); assigning a block index for the block of data the block index having a block index value (**figure 5 “LOGICAL MAPPING”; Table 1**); dividing the block index value by N for acquiring a quotient Q and a remainder R, wherein N is number of banks of the memory; identifying a physical address based on Q and R (**col. 6, lines 32 – 44; figure 5**) wherein the calculating step makes the block index interleaved at all times mapping to the physical address located at different unconnected banks and any two logically successive blocks of data be stored physically at different unconnected banks of the memory (**col. 6, lines 32 – 44**); storing the block of data in the memory at the physical address (**figure 5 “PHYSICAL MAPPING”**).

In regard to claim 12, Michigami teaches means for generating a block index for the block of data (**figure 5 “LOGICAL MAPPING”**); means for dividing a value of the block index by N for acquiring a quotient Q and a remainder R, wherein N is a number of

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banks of the memory (**col. 6, lines 32 – 44**); and means for calculating a physical address of the memory in which to store the retrieved block of data based on Q and R (**figure 5**), wherein the calculating means interleaves the block index at all times by mapping to the physical address to different unconnected banks so that any two logically successive blocks of data are stored at different unconnected banks of the memory (**col. 6, lines 32 – 44**).

In regard to claims 1, 6, 12, & 20, Michigami does not teach wherein the integer value is more than two, as cited in claim 1, or that the number of memory banks is more than two, as cited in claims 6, 12, & 20. However, interleaving to more than two banks is well known in the art, as shown by Hennessey (**page 432, figure 5.32**). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Michigami's invention by expanding the number of banks beyond two as this would optimize sequential memory accesses (**page 432, paragraph 2**).

Regarding claims 2, 7, 13, & 18, Michigami teaches wherein the memory supports pipelining access (**col. 4, lines 12 – 15**).

Regarding claims 3, 8, 14, & 19, Michigami teaches wherein the memory is a SDRAM (**fig. 4, element 18**).

Regarding claims 4, 9, & 15, Michigami teaches dividing the block index value by N to obtain a quotient Q and a remainder R (**col. 6, lines 32 – 44**); and calculating the physical address based on Q and R, wherein the physical address is calculated as the result of  $Q \times \text{block\_size} + R \times \text{bank\_size}$ , wherein bank\_size equals the memory size divided

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by N, and block\_size equals the size of which the system is in need to process one sector from the optical disc (**figure 5**).

Regarding claim 11, Michigami teaches reading the block of data according to the block index value and the reference function; (**figure 5**) and recording the block of data to a destination medium, whereby the reading includes reading each block of data from different memory banks in turns and to save processing by reducing pre-charge overloads by reading one bank and pre-charging another bank (**col. 6, lines 32 – 44; col. 5, lines 41 – 50**).

Regarding claims 21 - 22 & 24, Michigami teaches causing, while concurrently storing the block of data, a pre-charge for a memory bank other than the memory bank in which the block of data is stored (**col. 5, lines 41 – 50**).

Regarding claim 23, Michigami teaches retrieving a second block of data from the source medium (**Abstract**); assigning a second block index for the second block of data, the second block index having a second block index value (**figure 5 “LOGICAL MAPPING”; Table 1**);

dividing the second block index value by N for acquiring a quotient Q1 and a remainder R2, wherein N is a number of banks of the memory (**col. 6, lines 32 – 44; figure 5**); identifying a second physical address based on Q and R wherein the second block index is interleaved at all times and maps to a physical address located at different banks and any two logically successive blocks of data are stored at different banks of the memory(**col. 6, lines 32 – 44; figure 5**) ; and storing the second block of data in a second memory-bank of the memory at the identified second physical address

(**figure 5 “PHYSCICAL MAPPING”**) while concurrently causing a pre-charge for a first memory-bank in which the block of data was previously stored (**col. 5, lines 41 – 50**).

### ***Response to Arguments***

Applicant's arguments with respect to claims 1, 6, 12, & 20 have been considered but are moot in view of the new ground(s) of rejection.

### ***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

**Fung** (US 5,051,889) teaches interleaving multiple banks to omit the pre-charge cycle.

**Radke** (US 7,379,068) teaches precharging one memory while performing read or write operations on another.

**Oh** (US 7,345,940) teaches interleaving two or more banks so as to hide precharge time.

**Purcell** (US 7,275,126) teaches interleaving SDRAM memory banks to hide precharge and access time.



***Examiner's Information***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shawn Eland whose telephone number is (571) 270-1029. The examiner can normally be reached on MO - TH, & every other FR.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung Sough can be reached on (571) 272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Hyung S. Sough/  
Supervisory Patent Examiner, Art Unit 2188  
01/05/09

/Shawn Eland/  
Examiner, Art Unit 2188  
1/6/2009